

(d) forming a photoresist masking layer on portions of the MOS transistor structures where cobalt salicide regions are to be formed;

(e) removing the capping layer and the cobalt layer from those MOS transistor structures where cobalt salicide exclusion regions are to be formed;

(f) after step (e), stripping the photoresist masking layer; and

(g) after step (f), reacting cobalt in the cobalt layer with silicon in the exposed silicon surfaces to form cobalt salicide regions, wherein

step (b) includes the step of controlling at least one metal deposition parameter such that the cobalt layer has at least one predetermined property that causes the reaction of the cobalt with the silicon during step (g) to occur in a source limited manner and limits cobalt salicide crawl during step (g) beyond at least one of the portions of the MOS transistor structures where cobalt salicide regions are to be formed.

REMARKS:

Claims 1-13 have been finally rejected under 35 U.S.C. 103(a), as being unpatentable over U.S. Patent 6,087,227 (Hsu) in view of U.S. Patent 6,197,646 (Goto). In response, Applicant respectfully contends that these claims are patentable over the cited art for the following reasons.

Hsu fails to teach or suggest controlling a parameter of deposition of metal layer 430 (or any other metal deposition parameter) such that metal layer 430 (or another deposited metal layer) has a predetermined property that causes subsequent reaction of the metal with silicon (to form metal salicide regions) to occur in a source limited manner and limits metal (e.g., cobalt) salicide crawl during formation of the metal salicide regions (as recited in amended claims 1 and 8), or depositing a metal layer having a predetermined thickness over an IC structure, then removing the metal layer from those MOS transistor structures where metal salicide exclusion regions are to be formed, and then reacting remaining portions of the metal layer with silicon of the MOS transistor structures to form metal salicide regions in a source limited manner (as recited in claim 13). The Examiner has not contended that Hsu includes such a teaching or suggestion.

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Rather, Hsu teaches away from the invention by teaching a conventional method in which more metal is deposited than will react during a subsequent salicide-forming reaction. Specifically, Hsu teaches at col. 6, line 65-col. 7, line 5, that unreacted metal 430 is removed (e.g., by dry etching) from over structures 410, 412, 414, 420 and 423 after a salicide-forming reaction, leaving salicide layers 450 exposed (as shown in Fig. 3F). Hsu's salicide layers 450 are not formed in a source limited manner, since metal over structures 416 (which are salicide exclusion regions) is available for forming salicide layers 450 and since there is more metal over structures 410, 412, 420, and 423 available for forming salicide than is actually used for forming salicide layers 450.

As explained in the specification, the claimed method can achieve the unexpected benefit of reducing salicide crawl over and under metal salicide exclusion regions (e.g., gate sidewall spacers) adjacent to a metal salicide region. Since metal is removed from locations where metal salicide exclusion regions are to be formed, there is only a limited amount of metal (i.e., the metal that remains after the removal step) available to form metal salicide regions in accordance with the invention. By controlling the thickness of the metal that remains after the removal step (by controlling the pre-removal step of depositing the metal), the metal salicide formation reaction is controlled and can be driven to completion (in the sense that the completion occurs when the limited amount of available metal is consumed by the reaction). The inventive salicide-forming reaction can thus be "source limited" in the sense that it is limited by the amount of metal available for reaction.

Goto teaches depositing metal (e.g., cobalt layer 11 Fig. 1D), and titanium nitride (TiN layer 12 of Fig. 1D) over the metal, over all regions of a semiconductor structure. A silicidation reaction is then performed before any of the metal is removed from over any portion of the structure where a salicide exclusion region is to be formed (in contrast with the method of claim 1, 8, or 13). Goto teaches at col. 9, lines 5-12, that metal salicide (e.g., salicide 11g, 11d, and 11s of Fig. 1E) is formed under the overlying titanium nitride layer, as shown in Fig. 1E. Then, as described at col. 9, lines 13-20, the titanium nitride (12) is removed and the unreacted metal (11) is then removed to produce a structure with exposed metal salicide (the structure shown in Fig. 1F). Then, an annealing operation is performed to lower the resistance of the metal salicide.

To form the Fig. 7A structure, Goto teaches (at col. 6) performance of operations similar to those described with reference Figs. 1D, 1E, and 1F. A continuous layer of metal (e.g., titanium or cobalt) is deposited over all regions of a semiconductor structure. A silicidation reaction (including two annealing stages) is then performed before any of the metal is removed from over any portion of the structure where a salicide exclusion region is to be formed (in contrast with the method of claim 1, 8, or 13). Then, as described at col. 6, lines 47-48, the unreacted metal is removed to produce the Fig. 7A structure which has exposed metal silicide 58.

When performing Goto's conventional metal salicide formation method, there is an effectively unlimited supply of metal available for forming salicide. There is no teaching or suggestion determinable from Goto that a limited amount of metal (i.e., metal remaining after a pre-silicidation reaction removal step) should be made available to form metal salicide regions, and that such limited amount of metal should have its thickness (or another of its parameters) controlled during deposition to drive a metal salicide formation reaction to completion (so that the reaction is source limited).

Goto fails to teach formation of metal salicide regions in a source limited manner as recited in claims 1, 8, and 13. If Goto's silicidation reaction were source limited, there would be no "residual" metal to be removed over the metal salicide regions after the reaction as described in Goto and shown in Goto's Fig. 1E.

Goto also fails to teach formation of metal salicide regions in a manner that limits metal (e.g. cobalt) salicide crawl, as recited in claims 1 and 8. The Examiner acknowledges that Goto "does not disclose reducing salicide crawl." However, the Examiner argues that the structure of Goto's Fig. 7A exhibits "no salicide crawl ... beyond the portions of the MOS transistor structure where metal salicide regions are to be formed." Applicant respectfully contends that the lack of apparent salicide crawl in Fig. 7A in no way implies that no such salicide crawl would result from implementing Goto's explicit teachings. There is no teaching or suggestion determinable from Goto that Fig. 7A is drawn to scale and is not a simplified drawing. The present application teaches that a conventional method such as

Goto's (in which a silicidation reaction is not source limited) would result in salicide crawl, and that such salicide crawl could be significantly reduced if the inventive method (in which the salicide-forming reaction is source limited) were performed rather than the conventional method. Since there is excess metal available during Goto's silicidation reaction and no metal removal (before the silicidation reaction) from over structures which are to be metal salicide exclusion regions, Goto's method would result in salicide crawl beyond the portions of a MOS transistor structure where metal salicide regions are to be formed.

Y There is no suggestion in either Goto or Hsu to control thickness of a deposited metal layer to form metal salicide regions in a source limited manner or to limit salicide crawl beyond the portions of a MOS transistor structure where metal salicide regions are to be formed. Goto's teaching at col. 10, lines 50-67 (with reference to Fig. 6A) regarding control of the thickness of a deposited metal layer is a teaching that the metal layer thickness affects the sheet resistance of the metal salicide that can be formed by silicidation and subsequent annealing. Goto teaches (at col. 10, line 60 to col. 11, line 4) that a sufficiently thick metal layer (thicker than 5 nm) should be used to achieve a desirably low metal salicide sheet resistance, since use of a thinner metal layer (thinner than 5 nm) would result in a higher metal salicide sheet resistance. Goto also teaches (at col. 10) that there should be a TiN layer over the metal layer (during silicidization), also to reduce sheet resistance of the resulting metal salicide.

This teaching does not amount to a teaching or suggestion to modify Hsu's method to reach the invention of claim 1, 8, or 13.

At col. 10, lines 45-50, Goto also teaches that the metal layer (deposited to implement Goto's method) should not have thickness so great that the silicidation process would destroy semiconductor junctions that are intended to underlie the metal salicide to be formed during the silicidation process. In the specific case that the "gate length is shortened to about 0.3 μ m or less," Goto teaches that the metal layer thickness should not exceed 15 nm to avoid "destruction of junctions at the salicide process."

This teaching does not amount to a teaching or suggestion to modify Hsu's method to reach the invention of claim 1, 8, or 13.

Applicant respectfully contends that there is no teaching determinable from Goto (or other art of record) that Hsu's method should be modified to reach the invention of claim 1, 8, or 13. Thus, Applicant respectfully contends that claims 1, 8, and 13 (and all claims depending therefrom) are patentable over Hsu and Goto, whether these references are considered individually or in combination.

Respectfully submitted,
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APPENDIX

Lines 10-13 on page 7 are hereby amended to read as follows:

accordance with the present invention have been performed. Silicon gates 120 and 122 (typical thickness being in the range between 1500 and 4000 angstroms) [overly] overlie the gate oxide layer 110 of MOS transistor structures 104 and 106, respectively. Silicon gates 120 and 122 can be made from either

Claims 1 and 8 are hereby amended to read as follows:

1. (Twice amended) A method for forming metal salicide regions and metal salicide exclusion regions during the manufacturing of an integrated circuit (IC), the method comprising the steps of:

- (a) providing an IC structure including a plurality of MOS transistor structures, the plurality of MOS transistor structures having exposed silicon surfaces;
- (b) depositing a metal layer on the IC structure in a controlled manner;
- (c) forming a photoresist masking layer on portions of the MOS transistor structures where metal salicide regions are to be formed;
- (d) removing the metal layer from those MOS transistor structures where metal salicide exclusion regions are to be formed;
- (e) after step (d), stripping the photoresist masking layer; and
- (f) after step (e), reacting metal in the metal layer with silicon in the exposed silicon surfaces to form metal salicide regions, wherein

step (b) includes the step of controlling at least one metal deposition parameter such that the metal layer has at least one predetermined property [, and the at least one predetermined property] that causes the reaction of the metal with the silicon during step (f) to occur in a source limited manner and limits metal salicide crawl during step (f) beyond at least one of the portions of the MOS transistor structures where metal salicide regions are to be formed.

8. (Twice amended) A method for forming cobalt salicide regions and cobalt salicide exclusion regions during the manufacturing of an integrated circuit (IC), the method comprising the steps of:

(a) providing an IC structure including a plurality of MOS transistor structures, the plurality of MOS transistor structures having exposed silicon surfaces;

(b) depositing a cobalt layer on the IC structure in a controlled manner;

(c) depositing a capping layer on the cobalt layer;

(d) forming a photoresist masking layer on portions of the MOS transistor structures where cobalt salicide regions are to be formed;

(e) removing the capping layer and the cobalt layer from those MOS transistor structures where cobalt salicide exclusion regions are to be formed;

(f) after step (e), stripping the photoresist masking layer; and

(g) after step (f), reacting cobalt in the cobalt layer with silicon in the exposed silicon surfaces to form cobalt salicide regions, wherein

step (b) includes the step of controlling at least one metal deposition parameter such that the cobalt layer has at least one predetermined property [, and the at least one predetermined property] that causes the reaction of the cobalt with the silicon during step (g) to occur in a source limited manner and limits cobalt salicide crawl during step (g) beyond at least one of the portions of the MOS transistor structures where cobalt salicide regions are to be formed.